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(54) CCD image sensor having reduced photodiode-to-photodiode crosstalk.

(57) A CCD image sensor comprising : (a) a first and a second linear arrays of individual imaging photodetectors aligned along a scanning line, each of the imaging photodetectors having a photodetecting aperture of a given width along the scanning line, a light shield having a width substantially equal to the width of the photodetecting aperture being provided between adjacent photodetecting apertures of both the first and second linear arrays so that adjacent photodetecting apertures in the first and second linear arrays are separated by a non-photodetecting area, the second linear array being offset from the first linear array along the scanning line by approximately the width of the photodetecting aperture of the photodetectors such that substantially all the light information applied between adjacent photodetecting apertures of the first linear array is sensed by photodetecting apertures of the second linear array ; (b) a first CCD register adjacent to the first linear array for receiving and storing the charge carriers generated by the imaging photodetectors of the first linear array ; and (c) a second CCD register adjacent to the second linear array for receiving and storing the charge carriers generated by the imaging photodetectors of the second linear array.

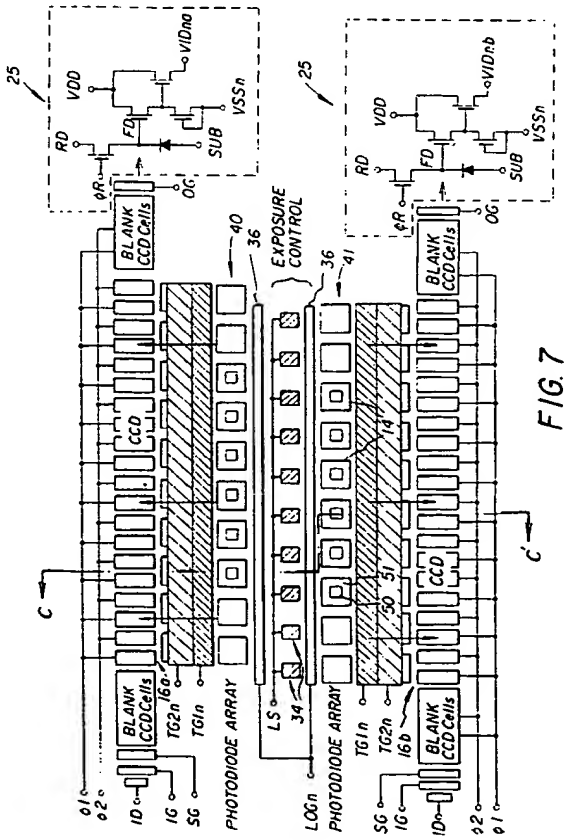

FIG. 7

EP 0 663 763 A2

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Field of the Invention

The invention relates to CCD image sensor and more particularly to an improved image sensor having ultra-high sampling abilities, low photodiode-to-photodiode crosstalk, high charge storage density, and electronic exposure control.

BACKGROUND OF THE INVENTION

Referring now to Fig. 1, there is shown a top plane schematic view of a conventional CCD imager. CCD imager 10 comprises a body of a semiconductor material having therein a plurality of imaging photodetectors 14. As shown, the imaging photodetectors 14 are arranged in an array of a line for a linear array. However, the photodetectors 14 can be arranged in an array of rows and columns for an area array. Each of the imaging photodetectors can be of any well known type of photodetectors, such as a photodiode or photocapacitor, which receives photons and converts the photons to charge carriers. Along one side of the line of imaging photodetectors 14 is a CCD shift register 16. CCD shift register 16 comprises a channel region (not shown) extending along and spaced from the line of photodetectors 14. If the channel region is a buried channel, it is a region of a conductivity type opposite that of the body of the CCD imager. A plurality of first gate electrodes 20 are over and insulated from the channel region. The first gate electrodes 20 are spaced along the channel region with each of the first gate electrodes 20 being adjacent a separate imaging photodetector 14. A plurality of second gate electrodes 22 are over and insulated from the channel region. The second gate electrodes 22 are arranged in alternating relation with the first gate electrodes 20 with each of the second gate electrodes 22 being adjacent a separate imaging photodetector 14. Thus there are two gate electrodes, one first gate electrode 20 and one second gate electrode 22 adjacent each imaging photodetector 14 to form a two-phase CCD shift register 16. The gate electrodes 20 and 22 are of a conductive material, such as conductive polycrystalline silicon, and are insulated from the channel region by a layer of an insulating material (not shown), typically silicon dioxide. The first gate electrodes 20 are all connected to a first clock phase $\Phi 1$ and the second gate electrodes are all connected to a second clock phase $\Phi 2$.

Transfer gates TGIn and TG2n extend over and are insulated from the body of the imager between the imaging photodetectors 14 and the channel region of the CCD shift register 16. Although two transfer gates are depicted here, it will be appreciated that only one transfer gate is really necessary. At the conclusion of an integration period, the collected photogenerated charges in each pixel are transferred to the adjacent CCD cell by applying the appropriate voltage biases to the TG1n and TG2n pins while the CCD remains in the idle state. At the conclusion of the charge transfer, the transfer gate clocks are returned to the isolation potentials and the CCD clocking resumes. As each charge packet is clocked over the OG potential at the end of the CCD, a corresponding change in output voltage at the VIDn pin of an output circuit 25 is observed.

A separate exposure drain region 34 is in the body of the imager, adjacent to, but spaced from the side of each imaging photodetector 14 opposite the CCD shift register 16. An exposure control gate 36 extends over and is insulated from the body of the imager between the imaging photodetectors 14 and the exposure drain regions 34. A potential is applied to the exposure control gate 36 (through pin LOGn) during a portion of the start of an integration period which lowers the potential barrier height between the imaging photodetectors 14 and the exposure drain regions 34. While the potential is applied, all charge carriers generated in the photodetectors 14 flow into the exposure drain regions 34 where they are carried away. After a desired period, the potential on the exposure control gate 36 is lowered, forming a barrier potential between the imaging photodetectors 14 and the exposure drain regions 34. This allows charges to be collected in the photodetectors 14 for the remainder of the integration period. Hence, the effective exposure time is limited to the duration while the exposure control gate potential is lowered. Such an electronic exposure structure is used in linear imagers containing multiple channels, each with a different color separation filter, to balance the photoresponse of each channel to the light source; thus achieving the maximum dynamic range in each channel (or color). The electronic exposure function is highly valued for multi-array linear imagers.

A more detailed description of the operation of CCD based solid state imagers can be found in J.D.E. Beynon, "Charge-Coupled Devices And Their Applications", McGraw-Hill, New-York, 1979 and M.J. Howes, "Charge-Coupled Devices and Systems" John Wiley and Sons, New-York, 1979.

One problem with the channel architecture shown in Fig. 1 is that for very small pixel pitch lengths (typically less than 9μm), several of the imager performance attributes are degraded. In particular, the Modulation Transfer Function (MTF) is decreased by the increase in photodiode-to-photodiode crosstalk and the charge density is reduced within the CCD by two-dimensional field effects. Such a problem of diffusion degradation of Modulation Transfer Function is depicted by David H. Seib in "Carrier Diffusion Degradation Of Modulation Transfer Function In Charge Coupled Imagers" in IEEE Transactions On Electron Devices, Vol. Ed 21, No. 3, March 1974 pp. 210-217. Also, for pixel pitch dimensions of less than 7μm, the layout dimensions shrink below fabrication design

limits.

Fig. 2 shows a bi-linear imager architecture which improves the charge storage density by allowing each CCD cell (20 & 22) to be two pixel pitch wide, as opposed to the one-to-one relationship in Fig. 1. To this end, transfer gates (TG1n and TG2n) along with their associated CCD shift registers (20 and 22) are provided on both sides of the imaging photodetectors 14. Via transfer gates TG1na, TG2na and TG1nb, TG2nb, the stored charges beneath each photosite 14 is transferred to their respective shift registers 16a and 16b. As can be seen from Fig. 2, all the odd photosites are coupled to shift register 16b and all the even photosites are coupled to shift register 16a. At the proper time, the information is shifted out to the right (or left) side of the device 10 to output circuits 25. Subsequent circuitry is then used to mix the outputs from circuits 25 such that the output pulse train is representative of the input applied light information. Such a structure has been used for example in the Kodak® KLI-5001 linear imager. However, this architecture does not include an electronic exposure circuitry and the layout design rules will again limit the pixel pitch dimensions, so that pitches less than 7μm cannot be reasonably obtained. Furthermore, such a structure suffers from increased photodiode-to-photodiode crosstalk for small pixel pitches, thus reducing the overall MTF.

Fig. 3 to which it is now made reference illustrates a slightly different version of the circuit shown in Fig. 2. According to this structure, the imager 10 is provided with an electronic exposure circuit (A) which has been added in the "gap" between adjacent transfer gate regions (TG1n and TG2n). Such an architecture has been used by Farchild® in the CCD181 linear imager. The problem with such a structure is that, as the pixel pitch becomes small (typically, less than 7μm), the above mentioned gap between adjacent transfer gate regions becomes too small to incorporate an electronic exposure structure. In addition, as for the structure of Fig. 2, this design suffers from increased photodiode-to-photodiode crosstalk for small pixel pitches, thus reducing the overall MTF.

Another approach is described in U.S. Patent No. 4,432,017 issued to Stoffel et al on February 14, 1984 as well as in IEEE International Solid State Circuits Conference; 1984; pp 36-37. This is illustrated in Fig. 4. The illustrated CCD array comprises a first row 40 of contiguous photosites and a second row 41 of contiguous photosites. The first row is contiguous with the second one. The second row 41 is offset from the first row of photosites by approximately one-half the length of photosites on the first row such that the second row of photosites is sensitive to light information applied between adjacent photosites of the first row. Shift registers 42, 43, 44 are provided adjacent to both first and second rows so as to collect the photogenerated charges, the output of registers 42 and 44 being multiplexed to generate a single output pulse train representative of the information scanned. As it appears from Fig. 4, there is no "non-photodetecting" area between two adjacent photodetecting apertures of a row as well as no "non photodetecting" area between the apertures of the first row and the adjacent apertures of the second row. Such a structure produces a substantial improvement in terms of aliasing. However, there is no improvement of the MTF. Furthermore, because of the photodiode-to-photodiode crosstalk which is a consequence of the close physical locations of the photodiode arrays, a less than ideal MTF is obtained. Last, such a design does not contain any electronic exposure capabilities.

A system similar with the same drawbacks is also described in U.S. Patent No. 4,712,137 issued to Kadekodi et al on December 8,1987.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide an improved CCD image sensor that overcomes the inadequacies mentioned in the above discussion with respect to conventional systems.

This object is achieved by providing a CCD image sensor comprising:

(a) a first and a second linear arrays of individual imaging photodetectors aligned along a scanning line, each of the imaging photodetectors having a photodetecting aperture of a given width along the scanning line for sensing light information applied thereon and converting the light information to charge carriers which are collected in a collecting area located under the photodetecting aperture;

(b) a light shield having a width substantially equal to the width of the photodetecting aperture being provided between adjacent photodetecting apertures of both first and second linear arrays so that in each of the first and second arrays, adjacent photodetecting apertures are separated by a non photodetecting area;

(c) the second linear array being parallel to the first array and offset from the first linear array along the scanning line by approximately the width of the photodetecting aperture of the photodetectors such that substantially all the light information applied between adjacent photodetecting apertures of the first linear array is sensed by photodetecting apertures of the second linear array;

(d) a first CCD register adjacent to the first linear array for receiving and temporarily storing the charge carriers generated by the imaging photodetectors of the first linear array; and

(e) a second CCD register adjacent to the second linear array for receiving and temporarily storing the charge carriers generated by the imaging

photodetectors of the second linear array.

These and other objects of the present invention will become more apparent when taken in conjunction with the following description and drawings wherein like characters indicate like parts and which drawings form a part of the present description.

The following are advantages of the present invention: it provides ultra-high spatial sampling, low photodiode-to-photodiode crosstalk, and high charge storage density. In addition it allows the incorporation of an electronic exposure structure.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 schematically represents the layout of a single channel of a linear imager as known in the PRIOR ART;

FIG. 2 shows the layout architecture of a single channel of another linear imager as known in the PRIOR ART;

FIG. 3 represents the layout architecture of another linear imager as known in the PRIOR ART;

FIG. 4 schematically represents the architecture of another device of the PRIOR ART;

FIG. 5 illustrates a first embodiment of the CCD imager of the invention;

FIG. 6 is an expanded view of the arrangement of the photodetectors in the CCD imager of FIG. 5;

FIG. 7 represents the layout architecture of a preferred embodiment of the CCD imager of the invention;

FIG. 8 shows another representation of the CCD imager of Fig. 7;

FIG. 9 represents another embodiment of the CCD imager of the invention; and

FIG. 10 is a cross-section view along line CC' of the CCD imager shown in Fig. 7.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 5 to which it is now made reference represents a first embodiment of the CCD image sensor according to the invention. The general structure of the system is similar to the one described in the above mentioned U.S. patents. The CCD image sensor according to the invention comprises a first 40 and a second 41 linear arrays of individual imaging photodetectors 14 aligned along a scanning line SL. As shown in more detail in Fig. 6, the first array 40 corresponds to the array of even pixels (n+1, n+3, n+5, n+7, etc.), the second one 41 corresponds to the array of odd pixels (n, n+2, n+4, n+6, etc.). These photodetectors 14 sense light information applied thereon through a photodetecting aperture 50 and convert this light information to charge carriers. The charge carriers are collected in a collecting area located under the photodetecting aperture 50. As it appears from Fig. 6, adjacent photodetecting apertures of both first and second arrays are separated by a light shielding layer 51 so that two adjacent photodetecting apertures are separated by a non-photodetecting area. As a result, a very high aperture MTF can be obtained. Also, a low diffusion crosstalk between photodiodes of the arrays can be obtained.

According to another feature of the invention, the second linear array 41, parallel to the first one 40, is offset from the first one along the scanning line SL by a distance which is substantially equal to the width T_p of the photodetecting apertures 50 so that, with a non-photodetecting area 51 having substantially the width of the apertures 50, substantially all the light information applied between adjacent photodetecting apertures of the first array is sensed by photodetecting apertures of the second array, thus providing a continuous spatial coverage over the full image length to be scanned.

Advantageously, as shown in Figs. 5 and 6, in order to lower the crosstalk between photodiodes of the first array and photodiodes of the second array, the light shielding layer 51 is provided all around the photodetecting apertures so that the photodetecting apertures of the first array 40 are separated from the photodetecting apertures of the second array by a non-photodetecting area. Advantageously, besides this non-photodetecting area, a further non-photodetecting space T_w can be provided between the two linear arrays. For example, such a space could be as wide as four times the width of the photodetecting aperture. According to one embodiment, this space is efficiently used by implanting under this non photodetecting space a structure, such as a drain to further minimize crosstalk between first array 40 and second array 41, thereby effectively reducing the photosite-to-photosite crosstalk. Alternatively, an electronic exposure structure can be positioned within this space. This will be described hereafter in more detail. Such a design can accommodate very small pixel apertures, such as 5μm or less. The pitch of the photodetectors, i.e. the distance T_p, would be in this example 10μm.

The CCD image sensor according to the invention also comprises transfer gates (TG1na, TG2na, TG1nb, TG2nb) located on both sides of the photodetecting arrays for, as explained in the background of the invention, transferring the charge carriers generated by the photodetectors into the shift registers 16a and 16b. The first shift register 16a, adjacent to the first array 40 receives and temporarily stores the charge carriers generated by the imaging photodetectors of the first array 40. The second shift register 16b receives and temporarily stores the charge carriers generated by the imaging photodetectors of the second array 41. Output circuits 25 are provided at one of the ends of each of the shift registers 16a, 16b to collect, amplify and transfer the shifted signals to

an output device, multiplexing means (not shown) being used to combine the signals issued from output circuits 25, so as to provide the information related to the full line being scanned.

Fig. 7 represents a imager which slightly differs from the one shown in Fig. 5 in that an electronic exposure structure 34, 36 has been provided between the two linear arrays of photodetectors 40, 41. Such a structure is used for controlling the exposure of both photodiode arrays 40, 41. Typically, such a structure comprises two exposure control gates 36 adjacent to each photodiode array and exposure drain regions 34 located between the two exposure control gates 36. The diode portion of such an exposure control circuitry also provides photodiode-to photodiode crosstalk suppression from even-to-odd and even-to-odd photodiodes as described earlier. Such a structure, also shown in more detail in Fig. 8, is well known and accordingly does not need any more detailed description.

Fig. 9 illustrates another embodiment of the imager according to the invention and in which isolation regions, such as isolation diode fingers 60 have been provided between adjacent photodetectors in each of the arrays. Such isolation diodes collect diffusing photogenerated charges and thus reduce the photodiode-to-photodiode crosstalk between pixels within a photodiode array.

Fig. 10 to which it is now made reference represents a cross section view along line CC' of the imager of Fig. 7. Also shown in Fig. 10 is the channel potential of the imager during integration periods (continuous line) and during transfer periods (interrupted line). According to a preferred embodiment of the invention, the surface of the collection area 52 under the photodetecting apertures 50 is greater than the surface of the apertures. This improves the collection efficiency of the image sensor.

The invention has been described in detail with particular reference to certain preferred embodiments thereof, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention.

PARTS LIST

10	CCD imager
14	photodetectors
16	CCD shift registers
16a	CCD shift registers
16b	CCD shift registers
20	first gate electrodes
22	second gate electrodes
25	output circuits
34	exposure drain region
36	exposure control gate
40	first array of photodetectors
41	second array of photodetectors
42	shift registers
43	shift registers
44	shift registers
50	photodetecting aperture
51	light shielding means
52	collecting area
60	isolation diodes

Claims

1. A CCD image sensor comprising:
   (a) a first and a second linear arrays of individual imaging photodetectors aligned along a scanning line, each of said imaging photodetectors having a photodetecting aperture of a given width along said scanning line for sensing light information applied thereon and converting said light information to charge carriers which are collected in a collecting area located under said photodetecting aperture;
   (b) a light shield having a width substantially equal to the width of said photodetecting aperture being provided between adjacent photodetecting apertures of both said first and second linear arrays so that adjacent photodetecting apertures in said first and second linear arrays are separated by a non-photodetecting area;
   (c) said second linear array being parallel to said first array and offset from said first linear array along said scanning line by approximately the width of the photodetecting aperture of the photodetectors such that substantially all the light information applied between adjacent photodetecting apertures of said first linear array is sensed by photodetecting apertures of said second linear array;
   (d) a first CCD register adjacent to said first linear array for receiving and temporarily storing the charge carriers generated by the imaging photodetectors of said first linear array; and
   (e) a second CCD register adjacent to said second linear array for receiving and temporarily storing the charge carriers generated by the imaging photodetectors of said second linear array.

2. A CCD image sensor according to claim 1 wherein said light shield is provided all around said photodetecting apertures so that the photodetecting apertures in said first linear array are separated from 5 the photodetecting apertures in said second array by a non photodetecting area.

3. A CCD image sensor according to claim 1 wherein said imaging photodetectors have a collecting

area whose surface is greater than the surface of the 10 corresponding photodetecting aperture.

4. A CCD image sensor according to claim 1 further comprising an electronic exposure structure for controlling the light exposure of said first and second linear arrays, said electronic exposure structure being located between said first and second linear arrays.

5. A CCD image sensor according to claim 4 wherein said electronic exposure structure comprises:
   i) a first exposure control gate adjacent to said first linear array;
   ii) a second exposure control gate adjacent to said second linear array; and
   iii) an exposure control drain region between said first and second exposure control gates.

6. A CCD image sensor according to claim 1 wherein isolation regions are provided between adjacent individual imaging photodetectors of said first and second linear arrays, in order to collect diffusing photogenerated charges.

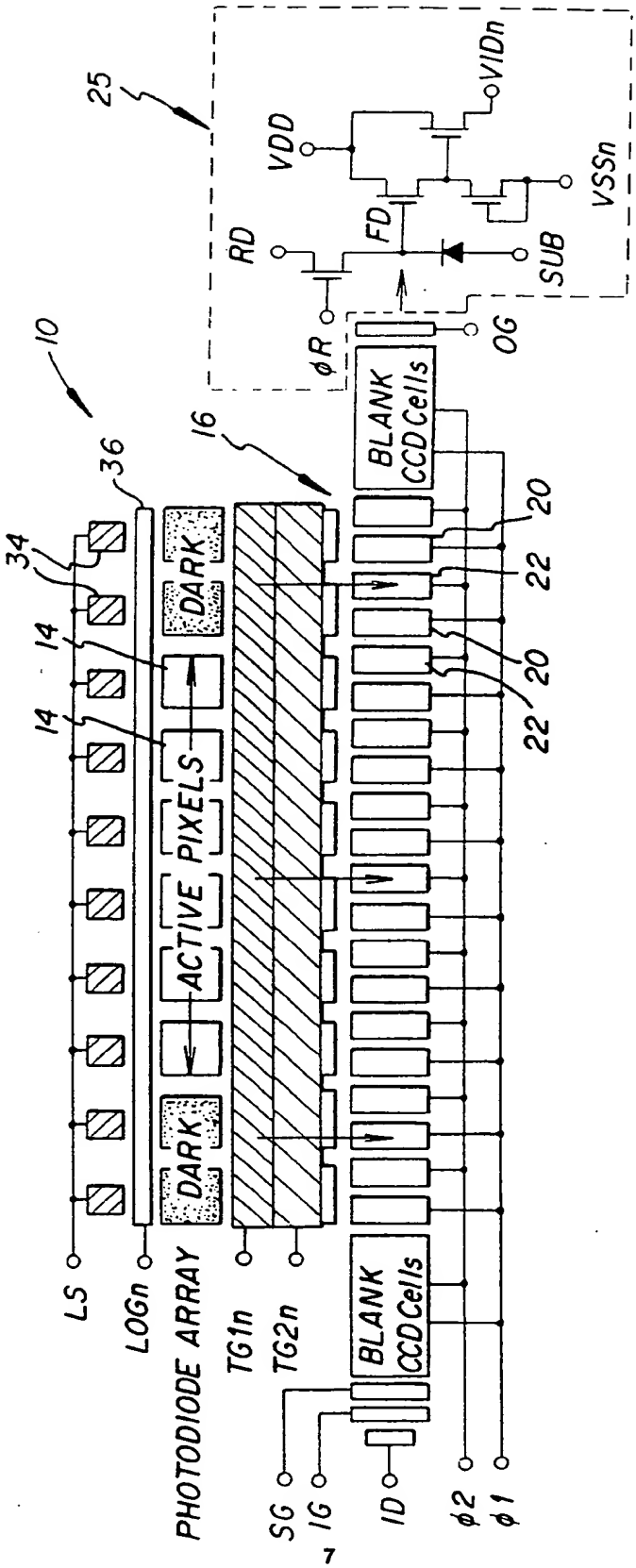

FIG. 1 (PRIOR ART)

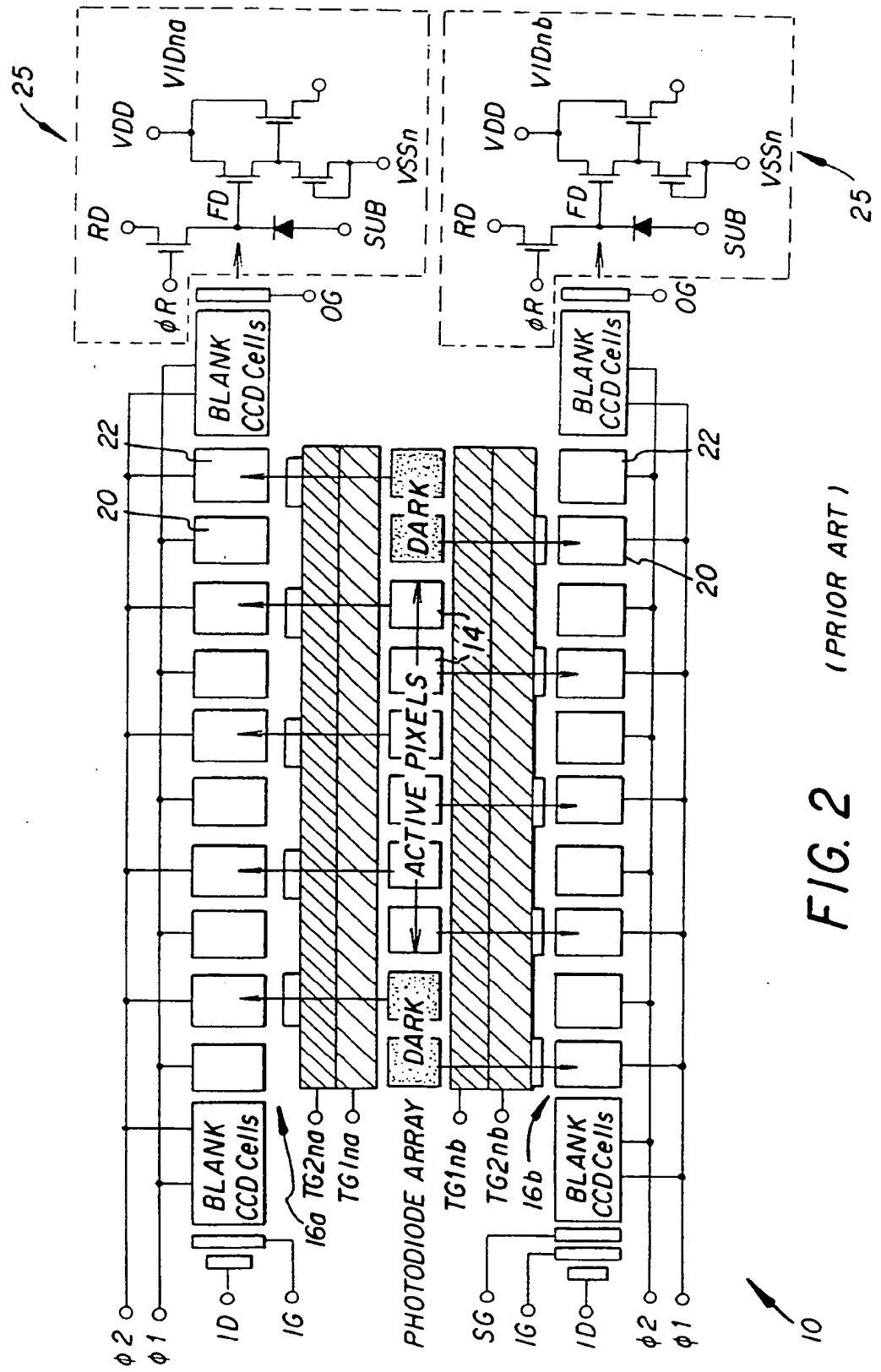

FIG. 2 (PRIOR ART)

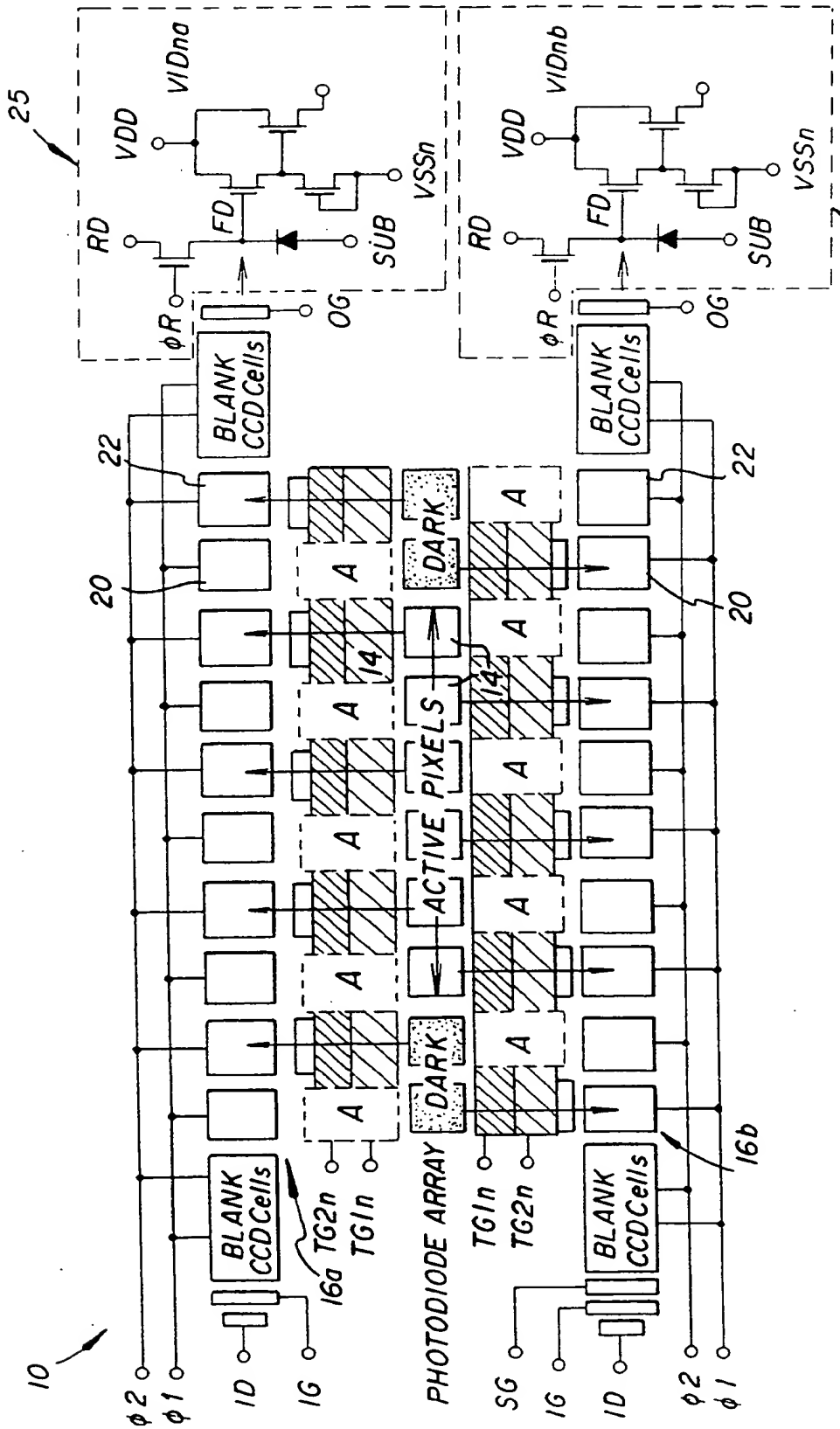

FIG. 3 PRIOR ART

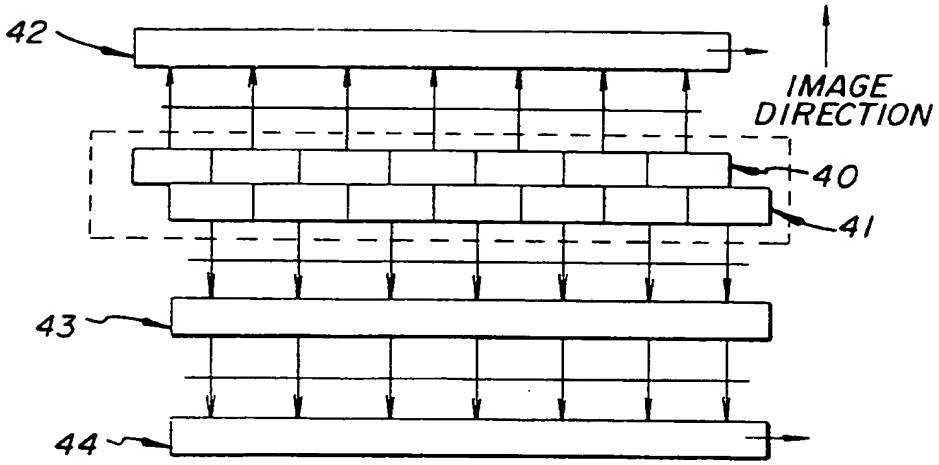

FIG. 4 (PRIOR ART)

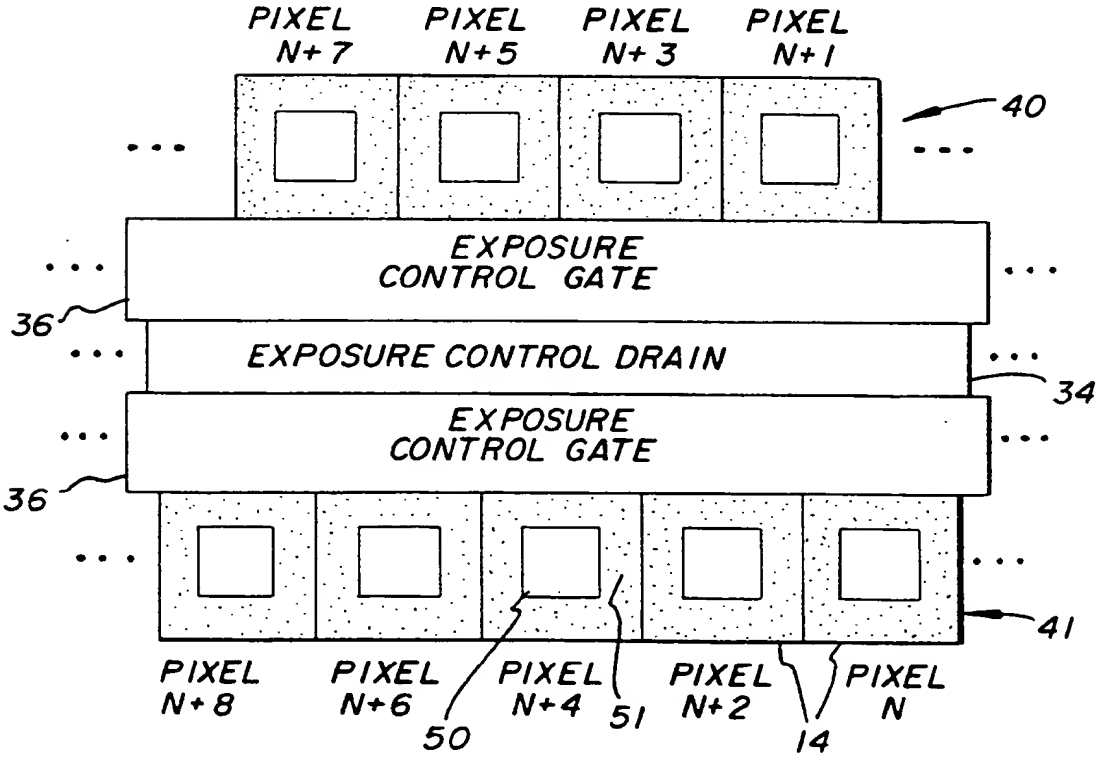

FIG. 8

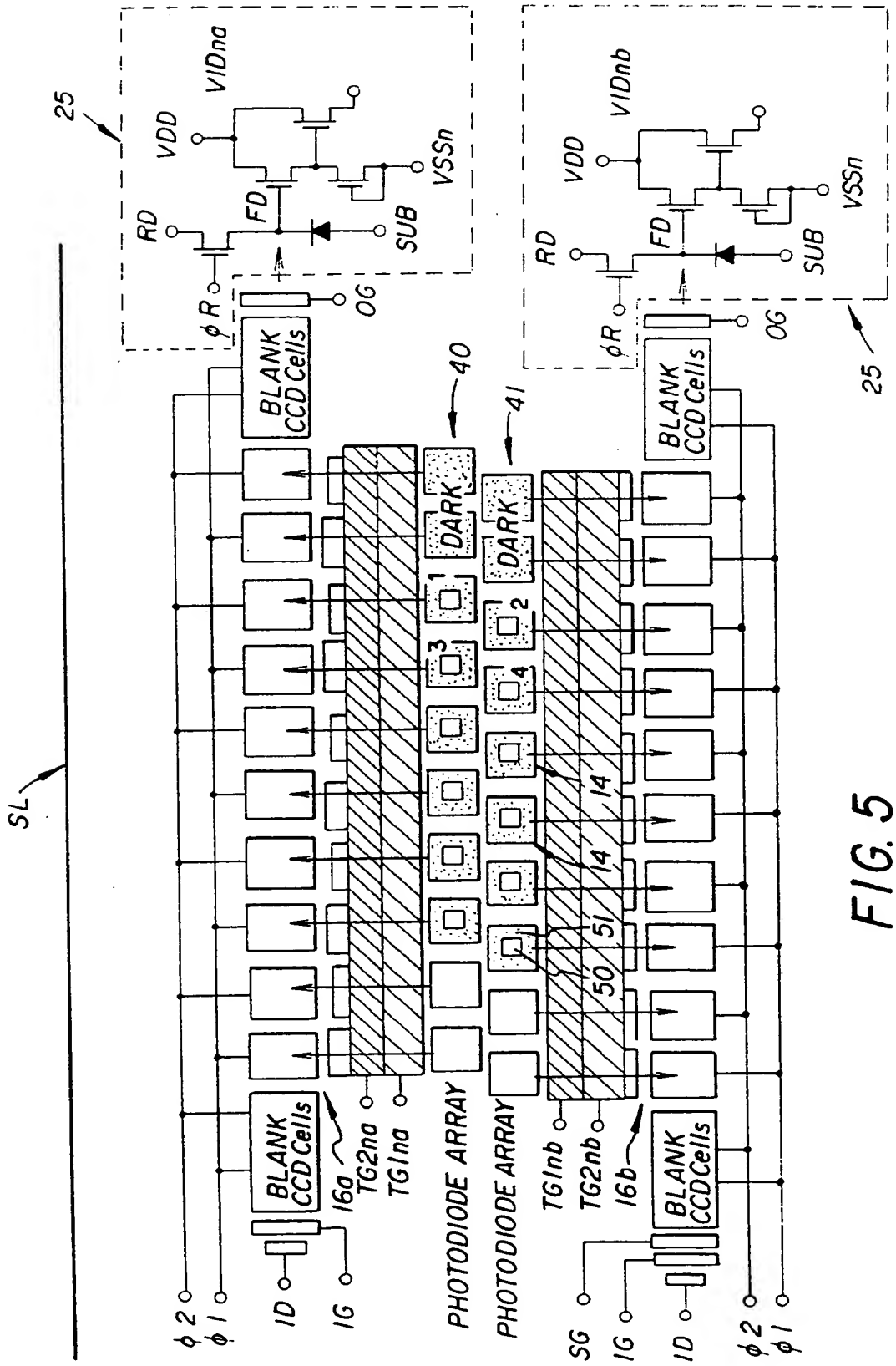

FIG. 5

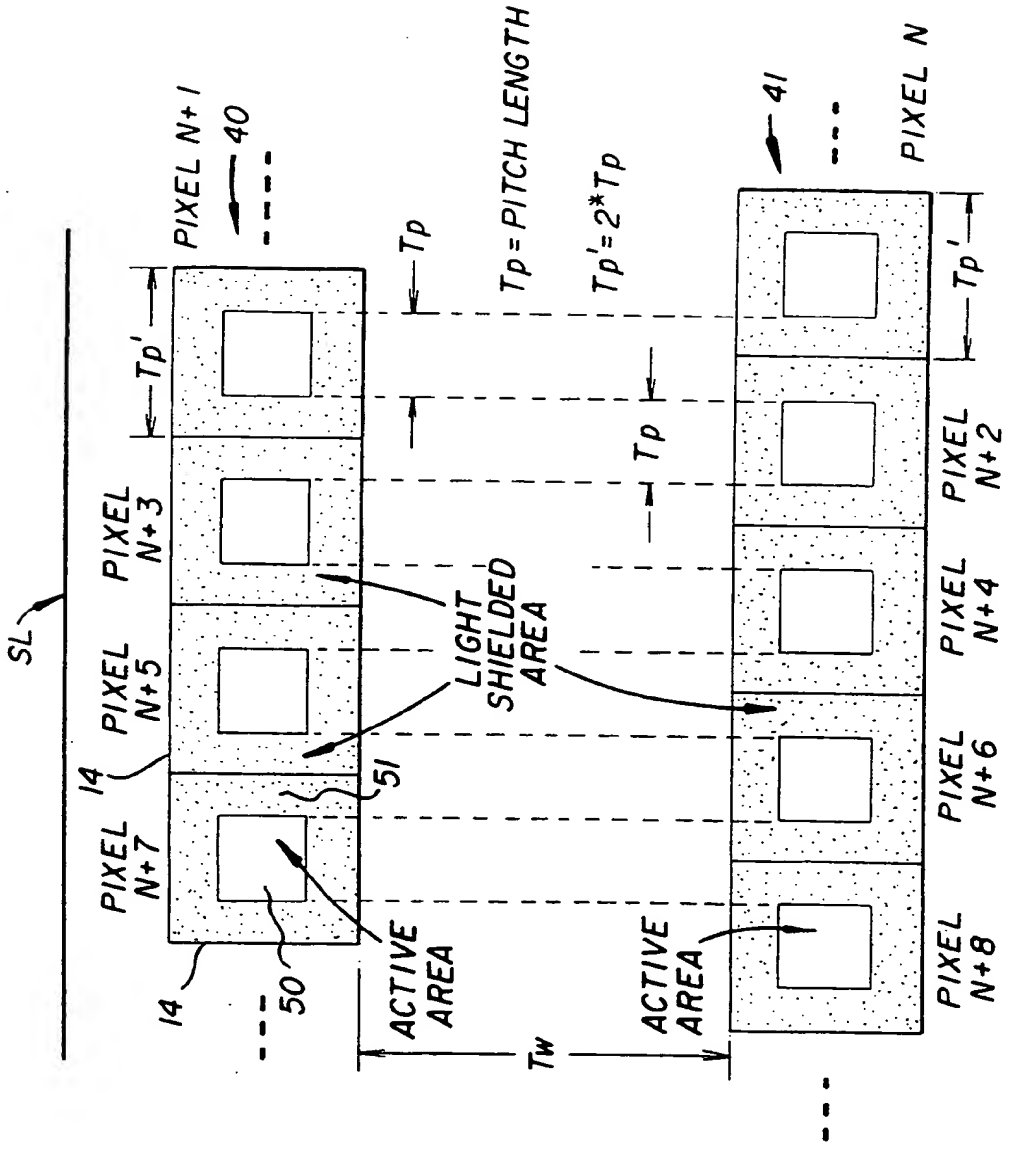

FIG. 6

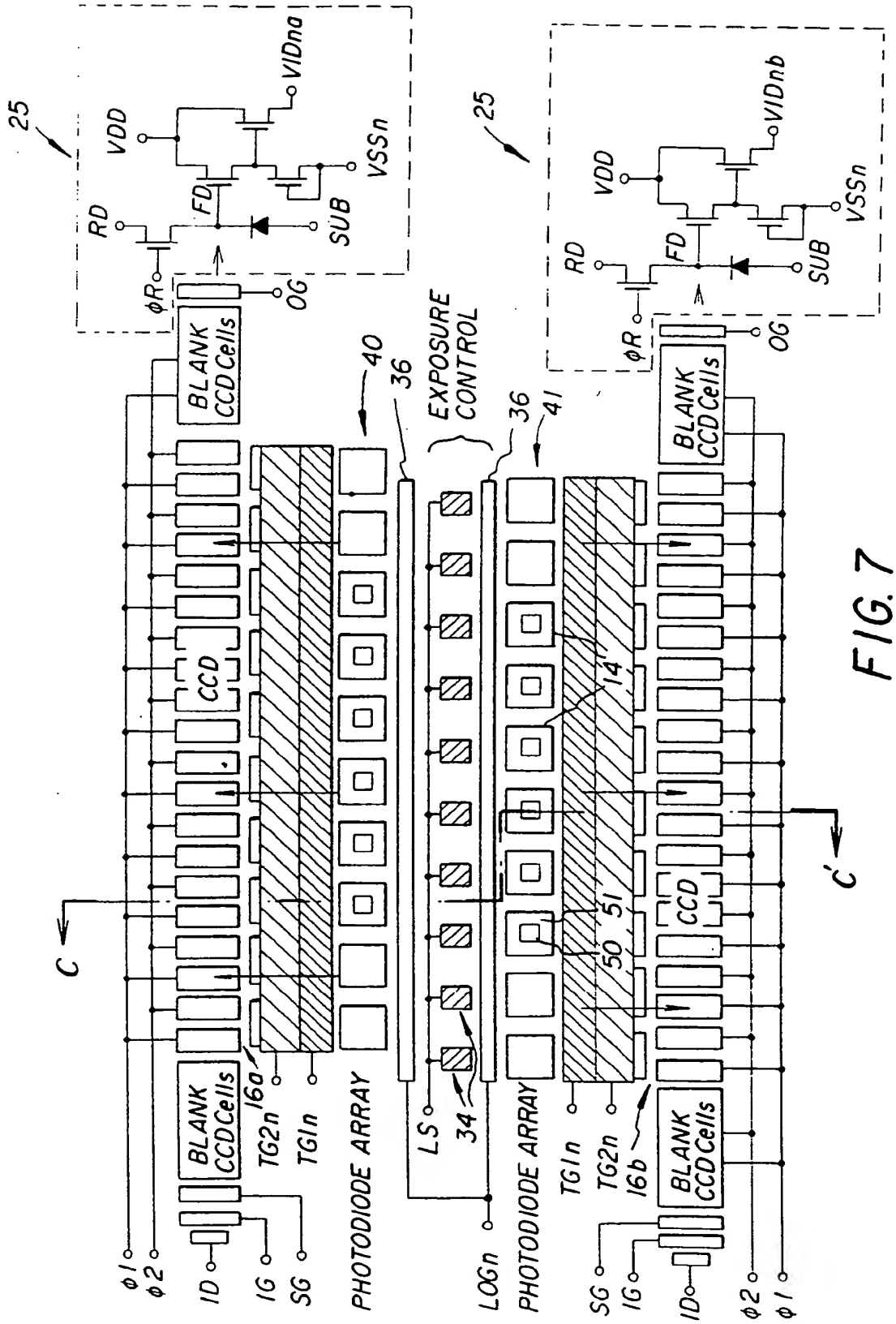

FIG. 7

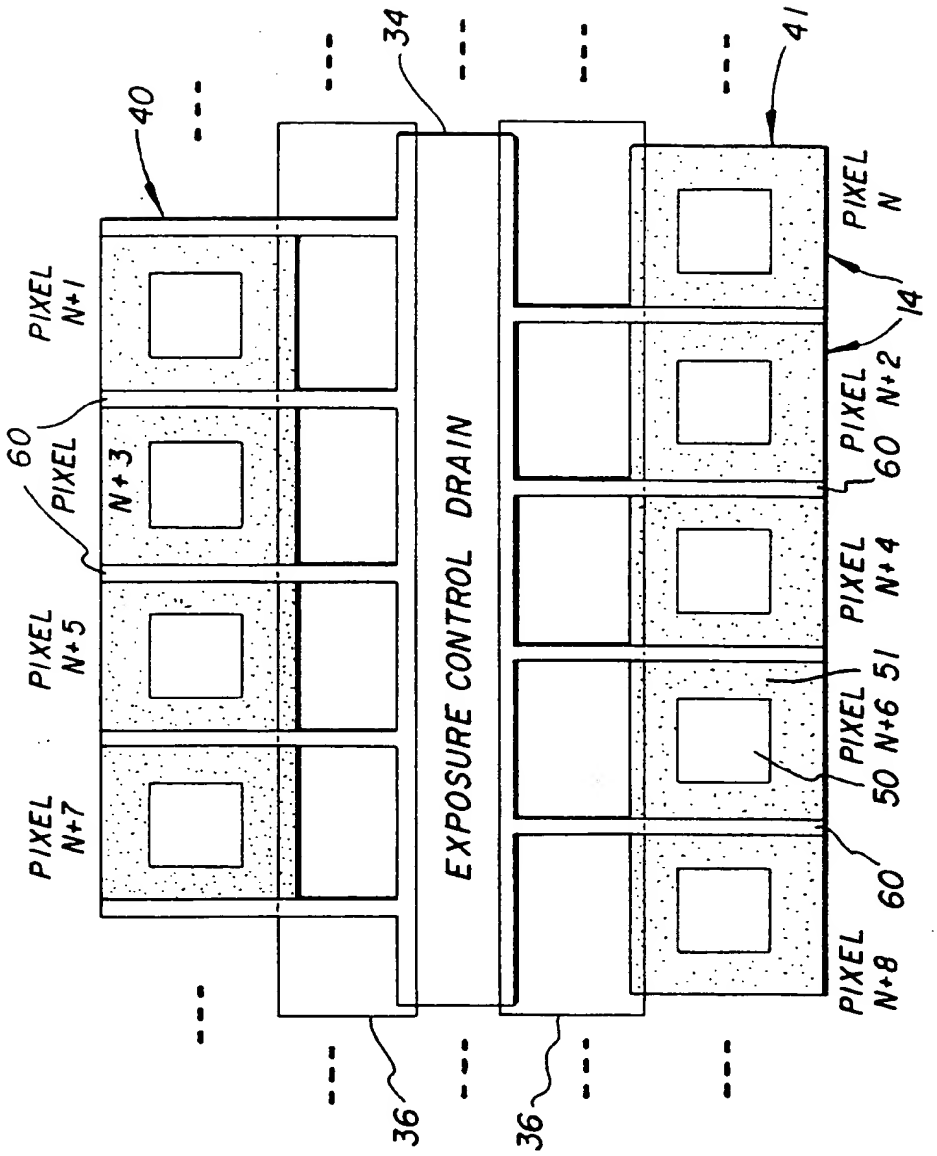

FIG. 9

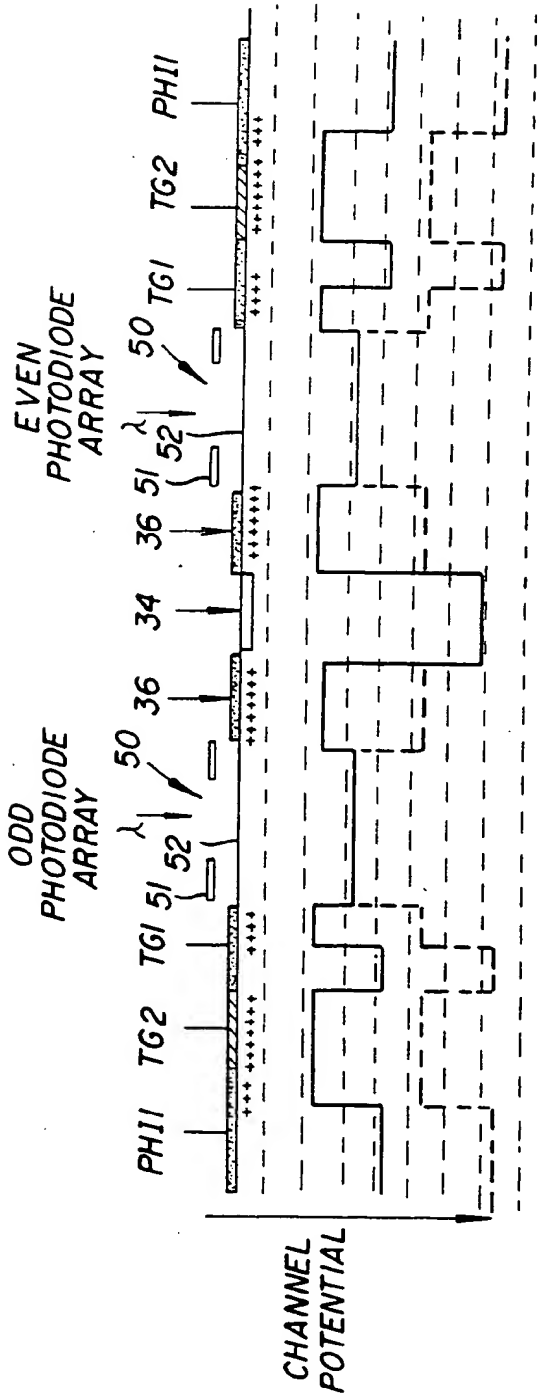

FIG. 10

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(54) CCD image sensor having reduced photodiode-to-photodiode crosstalk

(57) A CCD image sensor comprising: (a) a first and a second linear arrays of individual imaging photodetectors aligned along a scanning line, each of the imaging photodetectors having a photodetecting aperture of a given width along the scanning line, a light shield having a width substantially equal to the width of the photodetecting aperture being provided between adjacent photodetecting apertures of both the first and second linear arrays so that adjacent photodetecting apertures in the first and second linear arrays are separated by a non-photodetecting area, the second linear array being offset from the first linear array along the scanning line by approximately the width of the photodetecting aperture of the photodetectors such that substantially all the light information applied between adjacent photodetecting apertures of the first linear array is sensed by photodetecting apertures of the second linear array; (b) a first CCD register adjacent to the first linear array for receiving and storing the charge carriers generated by the imaging photodetectors of the first linear array; and (c) a second CCD register adjacent to the second linear array for receiving and storing the charge carriers generated by the imaging photodetectors of the second linear array.

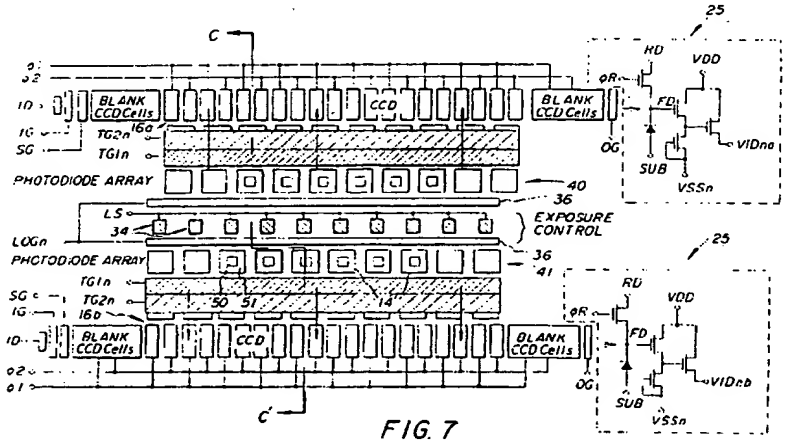

FIG. 7

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 42 0358

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	IEEE TRANSACTIONS ON ELECTRON DEVICES, vol. ED-32, no. 8, August 1985, NEW-YORK (US), pages 1541-1545, XP002028096 YUZUKI ET AL.: "A 5732-Element Linear CCD Image Sensor" * page 1542, left-hand column, line 11 - line 16 * * page 1542, right-hand column, line 27 - page 1543, left-hand column, line 1; figures 2C,,4 *	1-3	H04N3/15
Y		4-6	

Y	PATENT ABSTRACTS OF JAPAN vol. 006, no. 147 (E-123), 6 August 1982 & JP 57 069979 A (SANYO ELECTRIC CO LTD), 30 April 1982, * abstract *	4-6	

A	GB 2 152 328 A (ELTRO GMBH) 31 July 1985 * page 1, column 118 - page 2, column 3; figure 1 *	1	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
	---		H04N
A	EP 0 376 265 A (NIPPON ELECTRIC CO) 4 July 1990 * figure 2A *	1	

A	PATENT ABSTRACTS OF JAPAN vol. 007, no. 072 (E-166), 25 March 1983 & JP 58 001381 A (TOKYO SHIBAURA DENKI KK), 6 January 1983, * abstract *	1	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21 March 1997	Bequet, T

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